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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

760

APPL NUM 10027311	FILING DATE 12/21/2001	CLASS 324	SUBCLASS 718	GAU 2058	2133	EXAMINER <i>TRIMMING</i>
**APPLICANTS: Andreev Alexander; Vikhliantsev Igor; Ivanovic Lav;						
**CONTINUING DATA VERIFIED:						
** FOREIGN APPLICATIONS VERIFIED:						
PG-PUB	<input checked="" type="checkbox"/> DO NOT PUBLISH		<input type="checkbox"/> RESCIND			
Foreign priority claimed 35 USC 119 conditions met			<input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO 01-644 71742	
Verified and Acknowledged Examiner's initials						
TITLE : Built-in test for multiple memory circuits						
U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)						

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING		
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.	Print Fig.
TERMINAL DISCLAIMER		Primary Examiner		
		PREPARED FOR ISSUE		
		Application Examiner		
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